Applicant regards as the invention. These claims have been amended to eliminate extraneous references to the term "plurality of", as well as to clarify the Applicant's intent and to provide proper antecedent basis, according to the recommendations of the Examiner. In light of the amendments, the Examiner is asked to please note that the term "the circuit board" is correct as used in previous versions of the claims. The Applicant apologizes for any confusion on the part of the Examiner. No new matter has been added. The amendments, as well as all other amendments to claims 1-21, have been made solely to correct grammar and various informalities, as well as to clarify the Applicant's intent, and not for reasons related to patentability.

Rejections Under 35 U.S.C.§102

Claims 1, 2, 14-16, and 19 were rejected under 35 U.S.C.§102(e) as being anticipated by Farooq et al. (U.S. Patent No. 6,072,690); claims 1, 8, and 11 were rejected under 35 U.S.C.§102(e) as being anticipated by Naito et al. (EP 0 917,165 A2); and claims 1, 7, and 9 were rejected under 35 U.S.C.§102(b) as being anticipated by Watt (U.S. Patent No. 5,745,335). The Applicant respectfully traverses the rejection of these claims, and will demonstrate how the claim language distinguishes the instant invention over the cited art in the discussion which follows.

Farooq et al. In the Office Action, element 72 of Farooq et al. is characterized as both a "substrate" and an insulator layer. However, as illustrated in the instant application (Figure 1, elements 202 and 208, respectively), as well as in the Watt reference cited in the Office Action (Figure 1, elements 12 and 14, respectively), the substrate and dielectric are two distinct components. In the instant invention, the substrate is a layer through which conductive vias do not extend. Further, the substrate is not expected to contribute to the charge storage characteristics of the capacitor (otherwise why would a dielectric layer be formed over the substrate in Watt?). Thus, Farooq et al. does not disclose a substrate, *as claimed* in claims 1, 2, 14-16, and 19 by the Applicant.

Further, with respect to claims 2 and 15, it should be noted that it would be impossible to fabricate C4 lands "on" the third insulator layer, *as claimed* by the Applicant, using the embodiment disclosed by Farooq et al. in Figure 3C (see, for example, the illustration kindly

provided by the Examiner in the Office Action with respect to Naito, et al.). In addition, since there is no substrate from which to reference the conductive and insulator layers, there can be no "third" conductive layer upon which to fabricate C4 lands.

Finally, with respect to claim 16, the Office Action asserts Farooq et al. teaches that "the first integrated circuit package is a processor" in column 1, lines 11-45. The Applicant has carefully reviewed Farooq et al. and was unable to find a reference to a "processor". The Applicant respectfully requests that the location in Farooq et al. disclosing this element be cited with more precision.

Naito et al. In the Office Action, it is also asserted that Naito et al. discloses a substrate. However, Figure 1 of Naito et al. only recites and illustrates element 32, described as a "dielectric material layer". Such a continuous dielectric layer is not the same as a substrate, upon which dielectric material and conductive material may be formed. As discussed previously, a substrate is distinctly different from a dielectric layer. Thus, Naito et al. does not disclose a substrate, *as claimed* in claims 1, 8, and 11 by the Applicant.

Further, with respect to claim 8, the same difficulty arises with assigning the designation of a "second conductive layer" to any of the layers illustrated by Naito et al. (as described previously for Farooq et al.). Also, since there is no substrate shown, there can be no "second" conductive layer.

Watt The Office Action asserts that "Watt discloses in Figure 1 a ... substrate (1,2); a first conductive layer 7 located over the substrate ...". However, as discussed previously, and shown in Figure 1 of Watt, a substrate is not the same as a dielectric layer. In this case, layer "2" (element 14) of Figure 1 is an insulation layer formed *over* a substrate (layer 1, element 12). Thus, the insulation layer is not a substrate, being separate and distinct from the substrate, and the conductive layer is not located "over" the substrate, as claimed by the Applicant. Thus, Watt does not disclose a conductive layer located "over" a substrate, *as claimed* in claims 1, 7, and 9 by the Applicant.

Further, with respect to claim 9, Watt does not disclose a "third plurality of conductive vias" as claimed by the Applicant. Referring to Figure 5 of Watt, as suggested in the Office

Action, the Applicant was unable to locate any "plurality of vias", nor the reference numbers 38+, 40+, and 46+ in the "third" drawing of Figure 5. The Applicant respectfully requests that the location of these elements in Watt be designated with more precision.

In summary, since Farooq et al., Naito et al., and Watt fail to disclose each and every element of the invention as claimed by the applicant, especially including a "first conductive layer located over the substrate", it is respectfully requested that the rejection of claims 1, 2, 7-9, 11, 14-16, and 19 under § 102 be reconsidered.

Rejections Under 35 U.S.C.§103

Claims 2-3 were rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0 917,165 A2) in view of Farooq et al. (U.S. Patent No. 6,072,690); claims 4-5, 13, and 21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0 917,165 A2); claims 6 and 10 were rejected under 35 U.S.C.§103(a) as being unpatentable over Watt (U.S. Patent No. 5,745,335) in view of Yach et al. (U.S. Patent No. 6,225,678); claim 12 was rejected under 35 U.S.C.§103(a) as being unpatentable over Naito et al. (EP 0 917,165 A2) in view of Yach et al. (U.S. Patent No. 6,225,678); claims 18 and 20 were rejected under 35 U.S.C.§103(a) as being unpatentable over Farooq et al. (U.S. Patent No. 6,072,690) in view of Yach et al. (U.S. Patent No. 6,225,678); and claim 17 was rejected under 35 U.S.C.§103(a) as being unpatentable over Farooq et al. (U.S. Patent No. 6,072,690). The Applicant respectfully traverses these rejections of the claims, and will demonstrate how the claim language distinguishes the instant invention over the cited art in the discussion which follows.

Claims 2-3: Naito et al. in view of Farooq et al. Neither Naito et al. nor Farooq et al. disclose a substrate, as discussed previously, and claimed by the Applicant. Thus no combination of these references can supply the defective element. Further, even were the defective element to be supplied, the Office Action assertion as to the obviousness of the combination is not supported by the references.

To establish a prima facie case of obviousness, the references themselves must provide a suggestion or motivation for combination. MPEP §2143.01. References must be considered in

their entirety, including parts that teach away from the claims. MPEP 2141.02. "Obvious to try" is not a proper standard for determining obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir., 1988). "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988).

While the purported reason to combine the references in this case is to "improve the external connections to electrical components", no difficulty in connecting to external electrical components is recited in either reference. Rather, Naito et al. merely seeks to reduce the ESL of the capacitor, and Farooq et al. attempts to transfer signals using low-K sheathing around conductors. Thus, no motivation to combine the references is provided.

Further, with respect to claim 2, as noted above, it would be impossible to fabricate C4 lands "on" the third insulator layer, *as claimed* by the Applicant, using the embodiment disclosed by Farooq et al. in Figure 3C. Since there is no substrate from which to reference the conductive and insulator layers, there can be no "third" conductive layer upon which to fabricate C4 lands.

Finally, the Office Action admits that Naito et al. fails to disclose "C4 lands in electrical contact with the plurality of vias" with respect to claim 2. Thus, it is impossible for Naito et al. to disclose C4 lands fabricated in staggered columns in Figure 2, as asserted in the Office Action with respect to claim 3.

Claims 4-5, 13, and 21: Naito et al. As discussed previously, Naito et al. fails to disclose the element of a substrate, as claimed by the Applicant. It is also admitted that Naito et al. fails to disclose $BaSrTiO_3$ as an insulator material. Since all of the claimed elements are not found in the reference, the Applicant assumes that the Examiner is taking official notice of the missing elements. The Applicant respectfully objects to such official notice using a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

Further, with respect to claim 5, it is admitted that Naito et al. fails to disclose metal conductors made of copper. Since all of the claimed elements are not found in the reference, the Applicant again assumes that the Examiner is taking official notice of the missing elements. The

Applicant therefore respectfully objects to such official notice using a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

Claims 6 and 10: Watt in view of Yach et al. The defects of Watt have been previously discussed, namely, that Watt fails to teach a conductive layer located "over" a substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Watt and Yach et al. references. Yach et al. is directed toward connecting multiple capacitors to form a matched array. Watt recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors using the mesa-configuration of Watt. In fact, Watt teaches away from such a combination, describing "custom arrays" (i.e. non-matched capacitors), as shown in Figures 5 and 6. Finally, no suggestion to combine the references is provided from the references themselves.

Claim 12: Naito et al. in view of Yach et al. The defects of Naito et al. have been previously discussed, namely, that Naito et al. fails to teach a substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Naito et al. and Yach et al. references. Yach et al. is directed toward connecting multiple capacitors to form a matched array. Naito et al. recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors out of the single capacitor which is the subject of Naito et al. Finally, no suggestion to combine the references is provided from the references themselves.

Claims 18 and 20: Farooq et al. in view of Yach et al. The defects of Farooq et al. have been previously discussed, namely, that Farooq et al. fails to teach a substrate, *as claimed* by the Applicant. Further, it is not appropriate to combine the Farooq et al. and Yach et al. references. Yach et al. is directed toward connecting multiple capacitors to form a matched array. Farooq et al. recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors out of the single capacitor which is the subject of Farooq et al. Finally, no suggestion to combine the references is provided from the references themselves.

Claim 17: Farooq et al. As discussed previously, Farooq et al. fails to disclose the element of a substrate, as claimed by the Applicant. It is also admitted that Farooq et al. fails to disclose $BaSrTiO_3$ as an insulator material. Since all of the claimed elements are not found in the reference, the Applicant assumes that the Examiner is taking official notice of the missing elements. The Applicant respectfully objects to such official notice using a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

In summary, since Farooq et al., Naito et al., Watt, and Yach et al. fail to disclose each and every element of the invention as claimed by the applicant, especially including a "first conductive layer located over the substrate", and since no motivation to combine the references has been provided, it is respectfully requested that the rejection of claims 2-6, 10, 12, 13, 17, 18, 20, and 21 under § 103 be reconsidered.

Double Patenting Rejection

The Applicant has been advised that if claim 4 is found to be allowable, claim 21 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. Claim 21 has been amended to be substantially different from claim 4. No new matter has been added. Given the amendment of claim 21, the concern expressed in the Office Action respecting this point are now considered moot.

Conclusion

Applicant respectfully submits that claims 1-21 are now in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Mark Muller at 210/308-5677 or the below signed attorney to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 17 day of August, 2001.

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Name

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Signature